REMARKS

In the Final Office Action dated January 12, 2006, claims 1-3, 5, 11-13, 15 and 23 were rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,854,717, by Minuhin (hereinafter Minuhin). Claims 6-8, 16-18, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Minuhin in view of US Patent Application 2003/0090339, by Yu et al. (hereafter Yu). Applicants note with appreciation that the Examiner indicated that claims 9-10 and 19-20 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. In this Response, no claims have been added, canceled, or amended. Accordingly, claims 1-3, 5-13, 15-20, and 23-24 will be pending after entry of this Response.

I. Rejection of the Claims Under 35 U.S.C. § 102(b)

In the Office Action, claims 1-3, 5, 11-13, 15 and 23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Minuhin. Applicants respectfully traverse these rejections. Claim 1 recites a circuit comprising:

> at least one delay element for receiving an input signal and for generating a time delay in said signal to produce a time-delayed signal;
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> calibration circuit, coupled to said delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, said calibration circuit comprising a control loop for receiving an output signal from said delay element and a reference signal and for generating a phase adjustment based on a phase difference between said output and reference signals; and
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> multiplier-summing circuit, coupled to said delay element, for multiplying at least one signal output from said delay element to produce at least one multiplied signal and for summing at least one multiplied signal to generate an equalized signal.

Applicants submit that Minuhin does not disclose, teach, or even suggest each recited feature of claim 1. For example, Minuhin does not disclose, teach, or even suggest a calibration circuit for calibrating said delay element so as to match a time delay to a predetermined time period, the calibration circuit comprising a control loop for receiving an output signal from a delay element and a reference signal and for generating a phase adjustment based on a phase difference between said output and reference signals, as required in claim 1.

The Examiner indicates that the delay control circuit 78 and the adaptive tap weight control circuit 92 of Minuhin is equivalent to the calibration circuit of claim 1. The Examiner further indicates that signals 30 and 166 of Minuhin are equivalent to the output signal from a delay element and a reference signal, respectively, of claim 1. Even if it is assumed for the sake of argument that the latter is correct, the delay control circuit 78 and the adaptive tap weight control circuit 92 of Minuhin are still not equivalent to the calibration circuit of claim 1 as the Examiner states.

As shown in FIG. 3 of Minuhin, the delay control circuit 78 receives only a single signal (signal 166 which the Examiner equates to the reference signal of claim 1). As such, the delay control circuit 78 does not receive an output signal from a delay element, as required in claim 1. Since the delay control circuit 78 receives only a single signal (reference signal), the delay control circuit 78 also does not generate a phase adjustment based on a phase difference between the output and reference signals, as required in claim 1.

FIG. 3 of Minuhin shows that the adaptive tap weight control circuit 92 receives two signals (signals 30 and 166 which the Examiner equates to the output and reference signals, respectively, of claim 1). Minuhin does not teach or suggest, however, that the adaptive tap weight control circuit 92 then generates a phase adjustment based on a phase difference between the output and reference signals, as required in claim 1. Rather, in relation to the adaptive tap weight control circuit 92, Minuhin states the following at column 6, lines 1-12:

> ...equalizer 24A of FIG. 3 further includes analog multipliers 82, 84, 86, 88 and 90 which multiply tap signals from associated tap locations between the filter sections 70, 72, 74 and 76 by tap weight signals provided by an adaptive tap weight control circuit 92. As discussed in the U.S. Pat. No. 5,650,954, the adaptive tap weight control circuit 92 adaptively adjusts the tap weights during operation of the equalizer 24A in response to the tap signals, samples provided by the sampler 28 (as shown in FIG. 1) by way of signal path 30 and sampling clock signals provided from a timing delay circuit 96 (shown in FIG. 1) by way of signal path 166.
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> [Emphasis added.]

As such, as described in Minuhin, the adaptive tap weight control circuit 92 provides tap weight signals to analog multipliers (82, 84, 86, 88 and 90). Also, no where in Minuhin is it taught or suggested that the adaptive tap weight control circuit 92 generates a phase adjustment based on a phase difference between the output and reference signals, as required in claim 1. Therefore, neither the delay control circuit 78 nor the adaptive tap weight control circuit 92 of Minuhin, alone or in combination, are equivalent to the calibration circuit of claim 1.

For the above reasons, Applicants submit that claim 1 is in allowable form. Claims 2-3, 5, and 23 are dependent upon claim 1 and allowable for at least the same reasons as claim 1.

Further, Minuhin does not disclose, teach, or even suggest each recited feature of claim 23. For example, Minuhin does not disclose, teach, or even suggest that the reference signal received by the calibration circuit comprises the input signal received by the at least one delay element, as required in claim 23. As shown in FIGS. 1 and 3 of Minuhin, the signal path 166 (which the Examiner equates to the reference signal of claim 1) does not comprise the input signal 22 received by a delay element 70.

Independent claim 11 is a method claim having limitations similar to claim 1. Accordingly, claim 11 is in allowable form for the same reasons as stated above for claim 1. Claims 12-13 and 15 are dependent upon claim 11 and allowable for at least the same reasons as claim 11.

II. Rejection of the Claims Under 35 U.S.C. § 103(a)

Claims 6-8, 16-18, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Minuhin in view of Yu. Claims 6-8 are dependent upon claim 1 and allowable for at least the same reasons as claim 1. Claims 16-18 are dependent upon claim 11 and allowable for at least the same reasons as claim 11.

Independent claim 24 recites a circuit comprising:

> at least one delay element for receiving a signal and for generating a time delay in said signal, said delay element comprising a transmission line and a means for adjusting capacitance for said transmission line for calibrating said delay element;
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> calibration circuit, coupled to said delay element, for calibrating said delay element so as to match said time delay to a predetermined time period; and

multiplier-summing circuit, coupled to said delay element, for multiplying at least one signal output from said delay element and for summing at least one multiplied signal to generate an equalized signal.

Applicants submit that neither Minuhin nor Yu, alone or in combination, disclose, teach, or even suggest each recited feature of claim 24. In regards to claim 6, 16, and 24, the Examiner stated that Figure 3 of Yu discloses a delay element having a transmission line (inductor L) and an adjustable capacitance means (switch S and capacitor C) such that an accurate delay time is provided.

Yu, however, relates to an integrated filter circuit for digitally controlling characteristics of inductor and capacitor to produce a controlled resonant frequency (*see* Abstract) and does not relate to time delay circuits. No where in Yu is it taught or disclosed that a transmission line in the integrated filter circuit comprises a delay element with a means for adjusting capacitance of the transmission line for calibrating the delay element, as required in claim 24. In fact, no where in Yu is a delay element for generating a time delay in a signal even mentioned. Applicants respectfully request that the Examiner cite the precise portions of Minuhin or Yu that disclose the limitations of claim 24.

For the sake of argument, even if Yu discloses a transmission line and a means for adjusting capacitance for the transmission line, there is no motive to combine Minuhin and Yu. The motive to combine the Minuhin and Yu references must be found in the references themselves and not in the present application. As stated above, Yu relates to an integrated filter circuit and does not relate to or even mention time delay circuits – as such, there is no motive to combine Yu with Minuhin.

Applicants are not submitting that a delay element is novel in itself, nor that a transmission line and a means for adjusting capacitance for the transmission line is novel in itself, but rather that the combination of the two as delineated in claim 24 is novel. For the above reasons, Applicants submit that claim 24 is in allowable form.

III. Allowable Claims

Applicants note with appreciation that the Examiner indicated that claims 9-10 and 19-20 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. These claims are not being rewritten at this time, however, as Applicants believe the base claims on which these claims depend upon are in allowable form.

CONCLUSION

Based on the foregoing remarks, Applicants believe that the application is in condition for allowance. If the Examiner has any questions regarding the case, the Examiner is invited to contact Applicants' undersigned representative at the number given below.

Respectfully submitted,

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